ECR #: 3
Title: AGP-2X Mode Input Levels
Release Date: Nov. 15, 1996
Impact: Change
Spec Version: A.G.P. 1.0

Summary:

Change the 2X input levels to PCI 3.3 V specs.

Background:

ASIC foundry designers get better performance from single-ended (SE) input buffers than with differential buffers. The SE buffers do introduce more skew, but that is a design trade-off for the implementer. Timing will still be at $0.4*V_{DDQ}$ so no timing changes should be required in the spec.
Although the AGP-2X specs are set at the 1X levels, the spec for VREF remains for designs that use differential input buffers. Also, the spec will continue to recommend the use of differential input buffers to reduce the input sense range and input noise.

Change Current Specification as shown:

In table 4-2, change the VIL and VIH lines to match the VIL and VIH lines in table 4-1. I.e.:

Symbol	Parameter	Condition	Min	Max	Units	Notes
VIL	Input Low Voltage		-0.5	0.3*Vddq	V	
VIH	Input High Voltage		0.5*Vddq	Vddq + 0.5	V	